M TECH ELECTRONICS WITH SPECIALIZATION IN VLSI AND EMBEDDED SYSTEMS

Semester I

Course code	Name of course	C/E	Credits	Internal marks	External marks	Total
ELV3101/ SP 102	Advanced Digital System Design	C	3	50	50	100
ELV3102	**V**LSI Technology & Design	C	3	50	50	100
ELV3103	Designing with Microcontrollers	C	3	50	50	100
ELV3104	VLSI Design Automation	E	3	50	50	100
ELV3105	Embedded and Real Time Systems	E	3	50	50	100
ELV3106	System on chip design	E	3	50	50	100
ELV3107	Computer Communication Networks	E	3	50	50	100
ELV3108	Re configurable Computing Lab	C	1	100		100
ELV3109	RTOS Lab	C	1	100		100

Semester II

Course code	Name of course	C/E	Credits	Internal marks	External marks	Total
ELV3201	Analog Integrated Circuit Design	C	3	50	50	100
ELV3202	Advanced DSP Concepts and Architectures	C	3	50	50	100
ELV3203	Embedded System Design	C	3	50	50	100
ELV3204	Low power Digital design	E	3	50	50	100
ELV3205	High Speed Digital Design	E	3	50	50	100
ELV3206	CPLD & FPGA Architecture & Applications	E	3	50	50	100
ELV3207	Embedded LINUX Systems	E	3	50	50	100
ELV3208	Physical Design Lab	C	1	100		100
ELV3209	Advanced Microcontroller Lab	C	1	100		100
ELV3210	Seminar	C	1	50		50

Semester III

Course code	Name of course	Hours/week		Credits	Internal marks	External marks	Total
		L/T	P/S				
ELV 3301	Project Evaluation & Viva voce		30	18	100	200	300

Semester IV

Course code	Name of course	Hours/week		Credits	Internal marks	External marks	Total
		L/T	P/S				
ELV3401	Project Evaluation & Viva voce		30	18	100	200	300

ELV3101/ SP 102 ADVANCED DIGITAL SYSTEM DESIGN

Unit 1

MSI and LSI circuits and their applications: Arithmetic circuits, comparators, Multiplexers, Code Converters, XOR & AOI Gates, Design of sequential systems with small number of standard modules, State register Counters and RAM with combinational networks Multimodule implementation of sequential systems - Multimodule registers - and counters.

Unit 2

Sequential Circuit Design: Clocked Synchronous State Machine Analysis, Mealy and Moore machines, Finite State Machine design procedure – derive state diagrams and state tables, state reduction methods, and state assignments. Incompletely specified state machines. Implementing the states of FSM.

Unit 3

Asynchronous sequential circuits: Analysis, Derivation of excitation table, Flow table reduction, state assignment, transition table , design of asynchronous Sequential circuits, Race conditions and cycles, Static and dynamic hazards, Methods for avoiding races and hazards, essential hazards

Designing with SM charts – State machine charts, Derivation of SM charts, and Realization of SM charts.

Unit 4

Designing with Programmable Logic Devices: Read – Only Memories, Programmable Array Logic PALs, Programmable Logic Arrays PLAs – PLA minimization and PLA folding, Other Sequential PLDs, Design of combinational and sequential circuits using PLD's. Complex Programmable Logic Devices and Filed Programmable Gate Arrays - Altera Series FPGAs and Xilinx Series FPGAs

Unit 5

Timing issues in Digital system design: timing classification- synchronous timing basics – skew and jitter- latch based clocking- self timed circuit design - self timed logic, completion signal generation, self timed signaling–synchronizers and arbiters.

Text Book:

1. Charles H. Roth , *Fundamentals of Logic Design*, Thomson Publishers, 5th ed.
2. Milos D Ercegovac, Tomas Lang, *Digital systems and hardware / firmware algorithm*, John Wiley, 1985

References :

1. William I. Fletcher, *A Systematic Approach to Digital Design*, PHI, 1996.
2. N.N Biswas,*Logic Design Theory*, Prentice Hall of India, 1st Edn,1993.
3. Zvi Kohavi, *Switching and Finite automata Theory*, Tata Mc Graw Hill, 2nd ed.
4. Jan M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits- A Design perspective*, Pearson education/ Prentice-Hall India Ltd, 2nd ed
5. Comer, *Digital Logic State Machine Design*, Oxford University Press, 3rd ed.

ELV 3102 VLSI TECHNOLOGY & DESIGN

Unit 1

Review of Microelectronics and Introduction to MOS Technologies: Technology trends . MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. Mobility variation, tunneling, punch through, hot electron effect, Modelling of MOS transistors using SPICE.

Unit 2

Basic IC Processing Steps: Crystal growth and wafer preparation**,** epitaxy**,**Oxidation, Lithography, Etching techniques , film deposition, Diffusion, Ion implantation, metallisation, VLSI Process Integration NMOS, CMOS and BICMOS

Unit 3

Basics of Digital CMOS Design: The MOS Inverter: principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption. Latch-up in CMOS circuits. Ratioed logic, Pass Transistor logic, Arithmetic circuits in CMOS VLSI; Adders- multipliers-shifters.

Unit 4

Sequential MOS Logic Design: Static latches; Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design, SRAM and DRAM, Domino and NORA logic.

Unit 5

Circuit design Process : Circuit elements- resistor , capacitor, interconnects, sheet resistance , standard unit capacitance and unit delay concepts , inverter delays , driving capacitive loads, propagation delays, MOS layers, Stick diagrams and mask layout encoding, Design rules and layout, Lambda Based Design rules, micron based design rules, scaling of MOS circuits.

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, *CMOS Digital Integrated Circuits - Analysis & Design*, Tata MGH, 3rd edition.2003.
2. Douglas A Pucknell & Kamran Eshragian , *Basic VLSI Design*, PHI, Third Edition
3. S.M.Sze,*VLSI Technology*, McGraw Hill Book Company.

References :

1. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Pearson Education, Second Edition, 2003.
2. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000
3. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
4. Wayne, Wolf, Modern VLSI design: System on Silicon,Pearson Education,Second Edition.

ELV3103 DESIGNING WITH MICROCONTROLLERS

Unit 1

8-Bit Microcontrollers : Study of micro controller (MCS 51 family- 8051) -Architecture: CPU Block diagram, Memory organization, Program memory, Data memory, Interrupts, Peripherals: Timers, Serial port, I/O Port. Programming, Addressing Modes, Instruction Set, Programming, Comparison of various families of 8- bit Microcontrollers.

Unit 2

PIC 16F 87X Microcontroller: CPU Architecture - Block diagram ,Memory organization, Program memory, Data memory, Interrupts, Addressing Modes, Instruction Set , Peripherals: Timers, ADC , Serial port, I/O Port, Programming,

Unit 3

High Performance RISC Architecture : ARM

Background of ARM and ARM architecture versions V4, V5, V6, V7, ARM Cortex M3 archiecture , Programmers model , Thumb Instruction Set Architecture, Memory map, Exceptions, Clocking and resets, Power management, NVIC, Memory Protection Unit, Core Debug, System Debug, Cortex M3 development using the GNU tool chain.

Unit 4

Design, Development and Debugging Tools for Microcontroller based Systems: Software tools like Cross assembler, compiler, debuggers, simulators and hardware tools like In-Circuit Emulators(ICE), Emulators, Logic Analyzers etc.

Unit 5

Microcontroller based System Design: Case study with reference to a popular 8/16/32- bit microcontroller. A typical application design from requirement analysis through concept design, detailed hardware and software design using 8 ,16 and 32- bit Microcontrollers to demonstrate the use of Interrupts and available peripherals. Timing Analysis.

TEXT BOOKS

1. Ayala Kenneth J, *8051 microcontroller: Architecture, Programming and Application*, 1st edition, , West Publishing Company,1996.
2. John b Peatman, *Designing with Microcontrollers*, 1st edition, McGraw Hill International.
3. Muhammad Ali Mazidi,Janice G .Mazidi, R.D.Mckinlay, *The 8051 Microcontroller and Embedded Systems using Assembly & C*, 2nd Edition, Pearson Education

REFERENCES

1. *Embedded Microcontrollers*, 1st edition;by Intel Hand book.
2. Kenneth Hintz & Danniel, *Microcontroller Architecture, Implementation & Programming*", McGraw Hill, New york, 1992.
3. Predko, Myke *Programming and Customizing the 8051 microcontroller*", 1st edition,; McGraw Hill International.
4. Stewart, James W Miao, Kai X, *8051 Microcontroller: Hardware, software and Interfacing*, 2nd edition,
5. David Seal,*ARM Architecture Reference Manual* ,second edition Addison Wesley
6. Joseph Yiu ,*The Definitive Guide to the ARM Cortex- M3*, Newness.
7. *Cortex-M3 Technical Reference Manual* , ARM Limited.
8. *ARM v7-M Architecture Application Level Reference Manual*, ARM Limited
9. Andrew Sloss , Dominic Symes , Chris Wright ARM System Developer's Guide: Designing and Optimizing System Software (The Morgan Kaufmann Series in Computer Architecture and Design)

ELV3104 VLSI DESIGN AUTOMATION

Unit 1

Graph Algorithms: Data structures for Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm - Kruskal's and Prim's, Shortest path Algorithm - Dijkstra's and Bellman Fort Algorithm for single pair Shortest paths, Floyd-Warshall algorithm for All pair Shortest path, Matrix multiplication modeling of All pairs shortest path problem, Min cut and Max cut Algorithms

Unit 2

N-P complete Problem: Polynomial time non-deterministic algorithm, N-P completeness and reducibility, Proof and problems.

Logic synthesis & verification : Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis. Allocation , assignment and scheduling.

Unit 3

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction.

VLSI automation Algorithms:Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Unit 4

Placement, floor planning & pin assignment: problem formulation, placement algorithms, floor planning concepts, constraint based floor plannning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Unit 5

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

Detailed routing: problem formulation, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

Text:

1. Sabih H. Gerez, *Algorithms for VLSI Design* Automation, John Wiley & Sons, 1999
2. Naveed Shervani, *Algorithms for VLSI physical design Automation*, Kluwer Academic Publisher, Second edition.

References:

1. Christophn Meinel & Thorsten Theobold, *Algorithm and Data Structures for VLSI Design*, KAP, 2002.
2. Rolf Drechsheler ,*Evolutionary Algorithm for VLSI*, Second edition
3. Trimburger, *Introduction to CAD for VLSI*, Kluwer Academic publisher, 2002
4. T .H. Cormen, C. E. Leiserson, R. L. Rivest , *Introduction to Algorithms*, PHI.

ELV 3105 EMBEDDED AND REAL TIME SYSTEMS

Unit 1

Introduction to embedded systems: Categories of embedded systems, overview of embedded system architecture; specialties of embedded systems recent trends in embedded systems, Communication interfaces: RS232/UART RS 422/RS485, USB, IEEE1394, Bluetooth, Zigbee, Wifi, I2C, SPI, CAN, IDE, PCI, and Networking

Unit 2

Survey of software Architectures: Round Robin, Round Robin with interrupts, Function Queue scheduling Architecture, RTOS Architecture, Architecture selection, Introduction to RTOS,- Task and task states, Task and data, Semaphore and shared data, More operating system services, - Message Queues, Mail boxes and pipes, Timer functions , events, Memory Management, Interrupt routine in an RTOS environment.

Unit 3

Basic Design using an RTOS: Principle, Encapsulating Semaphores and Queues, Hard Real-Time scheduling considerations, saving memory space, saving power.

Unit 4

Embedded Software Development Tools:- Host and Target Machines, Linker/ Locator for Embedded Software , Getting Embedded Software into the target system, Debugging Techniques, Testing on your host machine, Instruction Set Simulators, The Assert Macro, Using Laboratory tools.

Unit 5

Writing Software for Embedded Systems:- The compilation process, Native versus cross compilers, Run time libraries, Writing a library, Using alternative libraries, Using a standard library, Porting Kernels, C extensions for Embedded Systems, Downloading, Emulation and Debugging Techniques, Buffering and other data structures, Linear buffer, Directional buffer, Double buffering, Buffer exchanging, Linked lists, FIFO, Circular buffers, Buffer under run and overrun, Allocating buffer memory, memory leakage, Memory and performance trade offs

TEXT BOOKS

1. Dr.K V K K Prasad, E*mbedded / Real time systems: Concepts, Design and Programming*, Dream Tech press, New Delhi, 2003.
2. David Simon, *Embedded Software Primer*, Addison- Wesley, 1999.

REFERENCES

1. Raj Kamal, *Introduction to Embedded Systems*, Tata McGraw Hill Publications, 2002.
2. Frank Vahid,Tony D. Givargis, *Embedded System Design- A Unified Hardware/ Software Introduction*, John Wiley and Sons, Inc 2002
3. Jonathan W. Valvano,*Embedded Microcomputer systems*, Brooks / Cole, Thompson Learning.
4. Arnold S Burger, *Embedded Systems Design - Introduction to Processes, Tools, Techniques*", CMP books.

ELV 3106 SYSTEM ON CHIP DESIGN

Unit 1

System On Chip Design Process: A canonical SoC Design, SoC Design flow - waterfall vs spiral, Top-down vs Bottom up, Specification requirement, Types of Specification**,** System Design process, System level design issues- Soft IP vs Hard IP**,** Design for timing closure, Logic design issues- Verification strategy, On-chip buses and interfaces, Low Power, Manufacturing test strategies.

Unit 2

Macro Design Process: Top level Macro Design**,** Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design process**,** System Integration with reusable macros.

Unit 3

Design for Testability Fundamentals:- Faults in Digital circuits. Fault models Digital test pattern generation – ATPG, Roth's D-algorithm, Vector Simulation- ATPG Vectors, Formats, Compaction and Compression., Scan Architectures and testing- , Generic Boundary scan, Full integrated scan, Syndrome test band signature analysis. Built in Self Test (BIST):-, BIST concepts and test pattern generation

Unit 4

SoC Verification:- Verification technology options,Verification methodology, Verification languages,Verification approaches,and Verification plans. System level verification, Block level verification,Hardware/software co-verification and Static net list verification .

Unit 5

MPSoCs: What, Why, How MPSoCs. Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design, MPSoC performance modeling and analysis. System-In-Package (SIP) design.

TEXT BOOKS

1. Prakash Rashinkar, Peter Paterson and Leena Singh, *SoC Verification-Methodology and Techniques*,.Kluwer Academic Publishers,2001.
2. Michael Keating, Pierre Bricaud,*Reuse Methodology manual for System-On-A-Chip Designs*,Kluwer Academic Publishers,second edition,2001.
3. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, *Digital systems Testing and testable Design*, Jaico Publishing House, 2001.

REFERENCES

1. William K.Lam, *Design Verification:Simulation and Formal Method based Approaches*,Prentice Hall.
2. Rochit Rajsuman, *System-on-a-Chip-Design and Test*,ISBN.
3. A.A.Jerraya, W.Wolf, *Multiprocessor Systems-on-chips*, M K Publishers.
4. Dirk Jansen,*The EDA HandBook*, Kluwer Academic Publishers.
5. Alfred Crouch, *Design for test for digital IC & Embedded Core Systems*, Prentice hall.
6. Stanley L. Hurst , *VLSI Testing: digital and mixed analogue digital techniques* ,Pub: Inspec / IEE, 1999

ELV 3107 COMPUTER COMMUNICATION NETWORKS

UNIT 1

Introduction to Data Communications and Networking:Introduction; Fundamental Concepts; Data communications; Protocols; Standards; Standards Organizations; Signal Propagation; Analog and Digital Signals; Bandwidth of a signal and a medium; The data transmission rate and thebandwidth. Modes of Data Transmission and Multiplexing :Introduction; Parallel and Serial Communication, Asynchronous, Synchronous and Isochronous Communication; Simplex,, Half-Duplex Communication, Multiplexing; Types of Multiplexing; FDM Versus TDM.

UNIT 2

Network Topologies, Switching and Routing Algorithms: Introduction; mesh Topology; Star Topology; Tree Topology; Ring Topology; Bus Topology; Hybrid Topology; Switching Basics; Circuit Switching; Packet Switching; Message Switching; Router and Routing; Factors Affecting Routing Algorithms; Routing Algorithms; Approaches to Routing.

UNIT 3

Asynchronous And Synchronous Transmission,Physical interfaces Transmission Errors: Detection and Correction: Introduction; Error Classification; Type of Error; Error Detection; Error control; Flow Control; Parity check, Longitudinal redundancy check, cyclic redundancy check, recovery from errors, CSMA.

UNIT 4

Networking Protocols and OSI Model: Introduction; Protocols in Computer Communications; OSI Model; OSI Layer Functions; Local Area Networks; Metropolitan Area Network; Wide Area Network.

UNIT 5

Network Security: Cryptography , Symmetric _key Algorithms, Public–Key Algorithms, Digital Signatures,Management of public keys. Communication Security, Authentications Protocols, E-mail Security, Web security, Social Issues.

Text Books:

1. Andrew S Tanenbaum , Computer Networks-,4th Edition. Pearson Education/PHI

References :

1. Michael A.Gallo, William M .Hancock, Computer Communications and Networking Technologies , Thomson Publication
2. Behrouz A. Forouzan, Data Communications and Networking, Third Edition TMH.
3. William Stallings , Data And Computer Communication , Prentice Hall, 4th Ed.
4. Srinivasan Keshav, Engg. approach to Computer Networking , Pearson Edu.

ELV 3108 RECONFIGURABLE COMPUTING LAB

HDL Programming using VHDL & Verilog – Combinational and Sequential circuit design , use of state machines, Compilation using Icarus verilog/ GHDL/ ISE or equivalent tools. Simulation using GTK wave/ Modelsim or equivalent tools.

Implementation of reconfigurable hardware for a variety of applications in signal processing – real time audio and video processing, high speed digital communication, embedded systems, etc.

ELV 3109 EMBEDDED OS AND RTOS LAB

Arrays, linked list, OS structures The kernel, Kernel structure, Kernel components and organization, Modes of operation, Booting and kernel initialization, Booting Basics, Boot-loaders (Various target specific boot loaders)etc. Device driver structure. Building a kernel from source, modifying an existing device driver, writing a new device driver, kernel debugging and testing and performance tuning. Writing and customizing device drivers for an embedded system. Kernel modules and kernel threads, Thread Design, Mutual Exclusion with Mutexes, Memory Management, Using Timing Facilities, Using Counting Semaphores for Event Notification, Synchronizing Threads with Event Flags Groups, Inter-Thread Communication with Message Queues, Priority Inversion, Preemption Threshold, Interrupts and I/O, Designing Multi-Threaded System etc.

ELV 3201 ANALOG INTEGRATED CIRCUIT DESIGN

Unit 1

Analog MOS transistor models – CMOS device models-MOS large signal model, small signal models, computer simulation models, subthreshold MOS models- SPICE simulation- . MOS diode/ Active Resistor, current sink/ sources – basics of single stage CMOS amplifiers - common Source, common gate and source follower stages - frequency response

Unit 2

CMOS Differential Amplifiers: CMOS Operational Amplifiers- one stage and two stage- gain boosting- Common mode feedback (CMFB) - Cascode and Folded cascade structures

Unit 3

High Performance Opamps – High speed/ high frequency op-amps, micro power opamps, low noise opamps and low voltage opamps. Current mirrors, filter implementations.

Unit 4

Supply independent and temperature independent references-Band gap references- PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits – effects due to non-linearity and mismatch in MOS circuits – Layout and packaging consideration for analog circuits – design rules – multi finger transistors – substrate coupling etc.

Unit 5

Switched Capacitor Circuits: First and Second Order Switched Capacitor Circuits, Switched Capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs- non ideal effects in PLLs, Delay locked loops and applications, basics of CMOS data converters – Medium and high speed CMOS data converters, Over sampling converters.

TEXT BOOKS

1. David. A. Johns and Ken Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, 2001.
2. Behzad Razavi, *Design of Analog CMOS Integrated Circuit*, Tata McGraw HILL, 2002.
3. Philip Allen & Douglas Holberg,"CMOS Analog Circuit Design", Oxford University Press, 2002.

REFERENCES

1. Paul B Gray and Robert G Meyer, *Analysis and Design of Analog Integrated Circuits*.
2. Behzad Razavi, *Principles of data conversion system design*, 2000. John Wiley
3. R Gregorian and G C Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley,1986.
4. R L Geiger, P E Allen and N R Strader, *VLSI Design Techniques for Analog & Digital Circuits*, McGraw Hill, 1990.
5. Gray, Wooley, Brodersen, *Analog MOS Integrated circuits*, IEEE press, 1989.
6. Kenneth R. Laker, Willy M.C. Sensen, *Design of Analog Integrated circuits and systems*, McGraw Hill, 1994.
7. Mohammed Ismail & Feiz , *Analog VLSI – Signal Information and Processing,*, John Wiley and Sons.

ELV 3202 ADVANCED DSP CONCEPTS AND ARCHITECTURES

Unit 1

Multirate system fundamentals: Basic Multirate operation – up sampling and down sampling, Time domain and frequency domain analysis, identities for multirate operations, Interpolator and decimator design, Rate conversion, Polyphase representation.

Unit 2

Adaptive Signal processing: Adaptive systems, Open and Closed Loop Adaptation, Adaptive Linear Combiner, Adaptive Algorithms and structures – LMS algorithm, Ideal LMS, Newton Algorithm and its properties, Sequential Regression algorithm, Advantages and disadvantages of adaptive recursive filters – LMS algorithm for recursive filters, Random search algorithms, Applications

Unit 3

Pipe lining and parallel processing- pipe lining of FIR filters, Parallel processing, pipe lining and parallel processing for low power, retiming- definitions and properties, solving system of inequalities, retiming techniques, unfolding- algorithm for unfolding, properties of unfolding, critical path, unfolding and retiming, applications folding- folding transformation, register minimization techniques, register minimization in folded architectures.

Unit 4

Systolic Arrays- Systolic array design methodology, FIR Systolic arrays, selection of scheduling vector, Matrix Matrix multiplications, 2 D systolic array design, Systolic design for space representations containing delays. Fast convolution – Cook Toom Algorithm, Winograd Algorithm, Iterated convolution, Cyclic convolution.

Unit 5

Synchronous, wave and asynchronous pipelines- Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs, Wave pipelining, asynchronous pipelining

Text Books:

1. Keshab K Parhi,VLSI DSP Systems- Design and Implementation – John Wiley, 2004.
2. P P Vaidyanathan ,Multirate Systems and filterbanks,, Prentice Hall, PTR.
3. Bernard Widrow & Samuel D. Streams Adaptive Signal Processing", , Prentice Hall.

References :

1. N J Fliege, Multirate Digital Signal Processing, John Wiley 1994.
2. John G Proakis and Dimitris G Manolokis, Digital Signal Processing Principles – Algorithms and applications", Prentice Hall, Third Edition,1999
3. Naim Dahnoun , Digital Signal Processing Implementation using the TMS320C6000 DSP Platform, 1st Edition
4. Rulf Chassaing, Digital Signal Processing and Application with C6713 and C6416 DSK,,Worcester Polytechnic Institute, A Wiley-Interscience Publication
5. Dan E. Dudgeson and Russel M, Mersereau, Multidimensional Digital Signal Processing, Prentice Hall.
6. Rulph Chassaing,DSP Applications using 'C' and the TMS320C6X DSK, 1st Edition
7. Andrew Bateman, Warren Yates, Digital Signal Processing Design, 1st Edition
8. James H. McClellan, Ronald Schaffer and Mark A. Yoder;DSP FIRST - A Multimedia Approach, 1st Edition; Prentice Hall
9. Digital Signal Processing- A Practical Approach", Emmanuel C Ifeachor, Barrie W. Jervis, Addison Wesley, 1993.

ELV3203 EMBEDDED SYSTEM DESIGN

Unit 1

Introduction : Embedded system overview,Design challenge: Optimizing design metrics, Processor Technology, General-purpose Processors, Single-purpose Processors, and Application Specific Processors, IC Technology: Full- custom/VLSI, Semi-custom ASIC, PLD, Trends, Design Technology.

Unit 2

Custom Single purpose Processor: RT- level combinational components, RT- level sequential components , Custom Single purpose Processor Design, RT- level Custom Single purpose Processor Design, Optimizing Custom Single- purpose Processors, Optimizing the original program, Optimizing the FSMD,Optimizing the datapath, optimizing the FSM.

General-purpose Processors: Basic architecture, Datapath ,Control unit, Memory, Pipelining, Superscalar and VLIW architectures. Application- Specific instruction-set Processors(ASIP's), Micro-controllers, DSP, Less- General ASIP environments, Selecting a Microprocessor/ General purpose Processor Design

Unit 3

Advanced Communication Principles: Parallel, serial and wireless Communications, Serial protocols: The I2C Bus, The CAN bus, Fire wire bus, USB. Parallel protocols: PCI bus, AMBA bus, wireless protocols: IrDA , Bluetooth, IEEE 802.11 .

Unit 4

Digital Camera Example: User's perspective, Designer's perspective, Specification, Informal Functional specification, Non-functional specification. Executable specification. Design, Implementation : 8051-based design, Implementation, Fixed point FDCT, Implementation, Hardware FDCT.

Unit 5

Control Systems: Open-loop and closed –loop control systems,an open-looped automobile cruise-controller,a closed-loop automobile cruise-controller,General control systems and PID controllers,Control objectives,Modeling real physical systems,Controller design,Fuzzy control. Practical Issues Related to Computer based Control,Benefits of Computer Based Control Implementations.

TEXT BOOKS

1. Frank Vahid and Tony Givargis , Embedded System Design-A Unified Hardware/Software Introduction",,John Wiley & Sons,2002.

REFERENCES

1. "Embedded System Design" Steve Heath, Butterworth Heinemann.
2. Gajski and Vahid, "Specification and Design of Embedded systems", Prentice Hall.

ELV 3204 LOW POWER VLSI DESIGN

Unit 1

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. Device & Technology Impact on Low Power, Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. Power estimation.

Unit 2

Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. **Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Unit 3

Low Power Design- Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. **Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, precomputation logic

Unit 4

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Unit 5

Low power Clock Distribution : Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock Network. **Algorithm & architectural level methodologies :** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text Books:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

References:

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000

ELV3205 HIGH SPEED DIGITAL DESIGN

Unit 1

Introduction to High Speed Digital Design:- Freequency, time and distance- Capacitance and Inductance Effects- High speed properties of logical gates- Speed and power- modeling of wires- Geometry and Electrical properties of wires- Electrical model of wires- transmission lines- lossless Lc transmission lines- lossy RLC transmission lines – Special transmission lines

Unit 2

Power Distribution and Noise:- - Power supply network-Local power regulation- IR drops- Area bonding- On chip bypass capacitors- Symbiotic bypass capacitors- Power supply isolation – Noise sources in digital system- Power supply Noise – Cross talk- Intersymbol interference.

Unit 3

Signalling convention and Circuits:- Signalling modes for transmission lines- Signalling over lumped transmission media- Signalling over RC interconnects- driving lossy LC lines- simultaneous bi-directional Signalling- terminators- transmitter and receiver circuits.

Unit 4

Timing Convention and Synchronisation:- Timing fundamentals- Timing properties of clocked storage elements- signals and events- open loop Timing , level sensitive clocking- pipeline Timing closed loop Timing – clock Distribution- Synchronisation failure and metastability- PLL and DLL based lock aligners.

Unit 5

Ultra fast VLSI Circuits and Systems: GaAs crystal structure, Technology development, Device modeling and performance estimation, Thermal design, Electromagnetic compatibility

Text Books:

1. Dally & Paulton ,Digital System Engineering, Cambride University Press,1998

Reference Books:

1. Johnson & Graham, High Speed Digital Design: A Handbook of Black Magic, Prentice Hall 1993
2. Masakazu Shoji, High Speed Digital Circuits, Addison Wesley, 1996
3. Jan M.Rabaey et al. Digital Integrated Circuits: A design Perspective, 2003

ELV 3206 CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

UNIT 1

Programmable logic : ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypres FLASH 370 Device Technology, Lattice pLSI's Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT 2

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs, Case studies – Xilinx Spartan-3, Virtex-II, Virtex-4, Virtex-5, Virtex-6 , Spartan-6 FPGAs & Sub-families, ALTERA's FLEX 8000/10000 FPGAs, NIOS II Ebbedded Processor, AT & T – ORCA's (Optimized Reconfigurable Cell Array), ACTEL's IGLOO series, ProASIC3 series FPGAs

UNIT 3

Finite State Machines (FSM): Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart suing microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties. Extended petrinetes for parallel controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT 4

FSM Architectures and Systems Level Design: Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT 5

Implementing Applications with FPGAs : Strengths and Weaknesses of FPGAs, Application and computational Characteristics and Performance - General Implementation Strategies for FPGA-based Systems - Configure-once Runtime Reconfiguration Design Flow – .Implementing Arithmetic - Fixed-point, Floating- point, Block Floating Point, Number Representation and Arithmetic Constant Folding and Data-oriented Specialization .Instance-specific Design - Distributed Arithmetic -

CORDIC Architectures for FPGA Computing - CORDIC Algorithm, Architectural Design, FPGA Implementation of CORDIC Processors .Guidelines and Case Studies of paraller adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers

TEXT BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.

References:

1. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
2. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
3. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
4. Reconfigurable Computing The Theory and Practice of FPGA based Computation Scott Hauck and Andre DeHon Morgan Kaufmann Publishers

ELV 3207 Embedded Linux Systems

Unit 1

Introduction: Embedded Linux, Real Time Linux,Types of Embedded Linux systems, Advantages of Linux OS, Using distributions, Examples of Embedded Linux systems- system architecture, Types of host/target architectures for the development of Embedded Linux Systems, Debug setups, Boot Configurations, Processor architectures supported by Linux

Unit2

Cross platform Development toolchain: GNU tool chain basics, Kernel Headers Setup, Binutils setup, Bootstrap Compiler Setup, Library Setup, Full Compiler Setup, Using the tool chain, C library alternatives, JAVA, Perl, Python, Ada, IDEs , Terminal Emulators

Unit3

Kernel and Root File System

Kernel Considerations- selection, configuration , Compiling and Installing the kernel Root File System Structure, Librariries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization

Unit4

Storage Device Manipulation

MTD-Supported Devices ,Disk Devices, Swapping

Root FilesystemSetup : Filesystem Types for Embedded Devices, Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem, Placing a Disk Filesystem on a RAM Disk , Rootfs and Initramfs, Choosing a Filesystem's Type and Layout, Handling Software Upgrades **Setting Up the Bootloader** Embedded Bootloaders, Server Setup for Network Boot,Using the U-Boot Bootloader

Unit 5

Device Drivers: Introduction, Building and running modules, Char Drivers,Allocating memory, USB Drivers, Device Model, Memory mapping and DMA, Block Drivers, TTY Drivers

Text Books:

1. Building Embedded Linux Systems **,** Karim Yaghmour, JonJason Brittain and Ian F. Darwin Masters, Gilad Ben-Yossef, and Philippe Gerum **,** O'Reilly
2. Linux Device Drivers , Alessandro Rubini, Jonathan Corbet, O'Reilly

Reference:

1. Embedded Linux Primer A Prctical Real – World Approch, Christopher Hallinan, Prentice Hall
2. Embedded Linux System Design and Development , P Raghavan, Amol Lad, Sriram Neelakandan , Auerbach Publications
3. Essential Linux Device Drivers , Alan Cox, Sreekrishnan , Venkateswaran , Pretice Hall
4. Embedded Linux Hardware, Software and Interfacing Craig Hollabaugh, Pearson Education

ELV3208 Physical Design Lab

Digital Integrated Circuit Design: Behavioral Modeling, RTL design, Synthesis, Verification, Placement, Routing, Design Rules, Layout Design, Parasitic extraction

Analog Integrated Circuit Design: Device Models, Spice simulation, Custom Layout Design

ELV3209 Advanced Micro controller Lab

8- bit Controller – Programming - use of IDEs - Interfacing examples
32- bit Controller – ARM – Programming- OS and RTOS – Kernel Porting – Writing Device Drivers.

ELV3210 Seminar