M. Tech. (VLSI and Embedded Systems)

Syllabus

Proposed Course Structure for M. Tech. (VLSI and Embedded Systems)

First Semester

Course Code	Name of Course	Internal Marks	Ext. Marks	Total Marks	C/E	Credits
ERD3101	Advanced Digital System Design	50	50	100	C	3
ERD3102	Advanced DSP	50	50	100	C	3
ERD3103	Analog VLSI	50	50	100	E	3
ERD3104	Electronic Design Automation Tools	50	50	100	E	3
ERD3105	Embedded and Real Time Systems	50	50	100	E	3
ERD3106	Designing with Microcontrollers	50	50	100	C	3
ERD3107	Design for Testability	50	50	100	E	3
ERD3108L	HDL Design and Implementation Lab	100	0	100	C	1
ERD3109L	VLSI Physical Design Lab	100	0	100	E	1
ERD3110L	High-Speed Design Lab	100	0	100	E	1

Second Semester

Course Code	Name of Course	Internal Marks	Ext. Marks	Total Marks	C/E	Credits
ERD3201	Seminar	100	0	100	C	2
ERD3202	System-On-Chip Design	50	50	100	E	3
ERD3203	VLSI-DSP Architectures	50	50	100	C	3
ERD3204	Embedded System Design	50	50	100	C	3
ERD3205	Advanced Microprocessor Architectures	50	50	100	E	3
ERD3206	VLSI Circuit Design and Technology	50	50	100	E	3
ERD3207	High Speed Digital Design	50	50	100	C	3
ERD3208	Electronic System Design	50	50	100	E	3
ERD3209L	Advanced Microprocessor Lab	100	0	100	C	1
ERD3210L	Embedded Systems Lab	100	0	100	C	1

Third Semester

Course Code	Name of Course	Internal Marks	Univ. Marks	Total Marks	C/E	Credits
ERD3301	Project Progress Evaluation	100	200	300	C	18

Fourth Semester

Course Code	Name of Course	Internal Marks	Univ. Marks	Total Marks	C/E	Credits
ERD3401	Project Dissertation Evaluation	100	200	300	C	18

ERD3101 ADVANCED DIGITAL SYSTEM DESIGN

Unit 1

MSI and LSI Circuits and their applications: Arithmetic circuits, Comparators, Multiplexers, Code Converters, XOR & AOI Gates, Wired Logic, Bus oriented structures, Tri-state bus system, Propagation Delay

Unit 2

Sequential Circuit Design: Clocked Synchronous State Machine Analysis, Mealy and Moore machines, Finite State Machine design procedure - derive state diagrams, obtain state tables, state reduction methods, state assignments. Incompletely specified state machines. Implementing the states of FSM

Unit 3

Designing with Programmable Logic Devices: Read-Only Memories, Programmable Array Logic PALs, Programmable Logic Arrays PLAs - PLA minimization and PLA folding, Other Sequential PLDs, Design of combinational and sequential circuits using PLD's.
XILINX FPGAs - Configurable Logic Block (CLB), Input/Output Block (IOB), Programmable Interconnection Points (PIP), XILINX CPLDs

Unit 4

Asynchronous sequential circuits: Derivation of excitation table, Race conditions and cycles, Static and dynamic hazards, Methods for avoiding races and Hazards, Essential hazards. Designing with SM charts - State Machine charts, Derivation of SM charts, and Realization of SM charts.

Unit 5

Advanced Topics In Boolean algebra: Shannon's Expansion Theorem, Consensus Theorem, Reed Muller Expansion, Design of static hazard free and dynamic hazard free logic circuits, Threshold logic, Symmetric functions.

TEXT BOOKS

1. "Fundamentals of Digital Design", Charles. H. Roth, Jr., PWS Pub. Co., 1998.
2. "Digital Design Fundamentals" Kenneth J Breeding, Prentice Hall, Englewood Cliffs, New Jersey. 1989**.**

REFERENCES

1. "A Systematic Approach to Digital Design", William I. Fletcher, PHI, 1996.
2. "Introduction to Digital Systems", James E. Palmer, David E. Perlman, Tata McGraw Hill, 1996.
3. "Logic Synthesis", S. Devadas, A. Ghosh and K. Keutzer, McGraw Hill, 1994.
4. "Logic Design Theory", N.N. Biswas, Prentice Hall of India, 1st Edn, 1993.
5. "Digital Design Principles and Practices", John F. Wakerly; Prentice Hall, 4th Edition, 2001.

ERD3102 ADVANCED DSP

Unit 1

Overview of one-dimensional DSP: Sampling of Continuous and Discrete signals, Z-Transform, DFT, FFT, Discrete Hilbert Transform, DWT. Design of FIR and IIR filters. Finite Word Length effects in signal processing.

Unit 2

Multirate system fundamentals: Basic multirate operation – upsampling and down sampling, Time domain and frequency domain analysis, Identities for multirate operations, Interpolator and decimator design, Rate conversion, Polyphase representation.

Unit 3

Adaptive Signal Processing: Adaptive systems, Open Loop and Closed Loop Adaptation, Adaptive Linear Combiner, Adaptive Algorithms and Structures – LMS algorithm, Ideal LMS / Newton Algorithm and its properties, Sequential Regression Algorithm, Advantages and disadvantages of adaptive recursive filters – LMS algorithm for recursive filters, Random search algorithms, Applications.

Unit 4

Multidimensional Signal Processing: 2-D Signals and Systems, Multidimensional sampling, Difference equations, Convolution, Fourier representation, Multidimensional FFT, Z-Transforms, Introduction to multidimensional digital filters

Unit 5

Signal Processing Hardware: General purpose Digital Signal Processors – Texas Instruments TMS320 family, Motorola DSP 56333 family, Analog devices ADSP 2100 family. Instruction set of TMS320C50 – simple programs. Real-time implementation considerations

TEXT BOOKS

1. "Multidimensional Digital Signal Processing", Dan E. Dudgeson and Russel M. Mersereau; Prentice Hall.
2. "Digital Signal Processing-A Practical Approach", Emmanuel C.Ifeachor, Barrie W.Jervis,, Addison Wesley, 1993.
3. "Adaptive Signal Processing", Bernard Widrow & Samuel D.Streams, Prentice Hall.

REFERENCES

1. "Digital Signal Processing", Defatta D.J., Lucas and Hodgkias, John Wiley and sons, 1995.
2. "Multirate systems and filter banks" P.P. Vaidyanathan, Prentice Hall. PTR.
3. "Multirate digital signal processing " N.J. Fliege. John Wiley 1994.
4. "The Scientist and Engineer's Guide to Digital Signal Processing" Steven W Smith.
5. "Digital Signal Processing Principles - Algorithms and Applications", John G. Proakis and Dimitris G. Manolakis; Prentice Hall, third edition, 1999.

ERD3103 ANALOG VLSI

Unit 1

Analog MOS Transistor Models - Temperature effects and Noise in MOS transistor- MOS resistors, characterization of resistive, capacitive elements and MOS devices- passive and active CMOS current sinks/sources- basics of single stage CMOS amplifiers- common source, common gate and source follower stages- frequency response.

Unit 2

CMOS Differential Amplifiers - CMOS operational amplifiers- one-stage opamps and two-stage opamps- gain boosting- common mode feedback (CMFB) - Cascode and Folded cascode structures

Unit 3

High Performance Opamps - High speed/high frequency op-amps, micro power opamps, low noise op-amps and low voltage opamps. Current mirrors, filter implementations.

Unit 4

Supply independent and temperature independent references- Band gap references- PTAT current generation and constant Gm biasing- CMOS comparators- multipliers and wave shaping circuits- effects due to non-linearity and mismatch in MOS circuits-Layout and packaging consideration for analog circuits- design rules- multi finger transistors- substrate coupling etc.

Unit 5

Switched Capacitor Circuits: First and second order switched capacitor circuits, switched capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs, non ideal effects in PLLs, Delay locked loops and applications, basics of CMOS data converters - Medium and High speed CMOS data converters, Over sampling converters.

TEXT BOOKS

1. "Analog Integrated Circuit Design", David A Johns & Ken Martin John Wiley and Sons, 2001.
2. "Design of Analog CMOS Integrated Circuit", Behzad Razavi, Tata-McGraw Hill, 2002.
3. "CMOS Analog Circuit Design", Philip Allen & Douglas Holberg, Oxford University Press, 2002.

REFERENCES

1. "Analog VLSI – signal information and Processing", Mohammed Ismail & Feiz, John Wiley & Sons.

ERD3104 ELECTRONIC DESIGN AUTOMATION TOOLS

Unit 1

Hardware Description Languages: Introduction to VHDL - Behavioral Modeling - Transport vs. Inertial Delay - Simulation Deltas - Sequential Processing - Process Statement - Signal Assignment vs. Variable Assignment - Sequential Statements - Data Types - Subprograms and Packages - Predefined Attributes - Configurations - Subprogram Overloading - VHDL synthesis - Design Examples

Unit 2

Synthesis and Simulation using HDLs: VHDL and logic synthesis – Memory synthesis, FSM synthesis, performance-driven synthesis. Simulation - types of simulation, logic systems, working of logic simulation, cell models, delay models state timing analysis, formal verification, switch-level. Simulation, transistor-level simulation. CAD tools for synthesis and simulation - ModelSim and Leonardo Spectrum

Unit 3

Tools for Circuit Design and Simulation using PSPICE: PSPICE models for transistors, A/D & D/A, sample and hold circuits etc, Digital system building blocks, design and analysis of analog and digital circuits using PSPICE.

Unit 4

An overview of Mixed Signal VLSI Design: Fundamentals of analog and digital simulation, mixed signal simulator configurations, understanding modeling, integration to CAE environments, analyses of analog circuits eg. A/D, D/A converters, up and down converters, Companders, etc.

Unit 5

Tools for PCB Design and Layout: An overview of high-speed PCB design, design entry, simulation and layout tools for PCB. Introduction to Orcad PCB design tools.

TEXTBOOKS

1. "VHDL analysis and Modeling of Digital Systems" Zainalabedin Navabi, University of Tehran, Mc Graw Hill, 1998.
2. "SPICE FOR Circuits And Electronics Using PSPICE (2/E)", M.H.RASHID, Prentice Hall, 1992.
3. "Application-Specific Integrated Circuits", M.J.S.SMITH. Addison Wesley

REFERENCES

1. ORCAD: Technical Reference Manual, Orcad, and USA.
2. SABER: Technical Reference Manual, Analogy Nic, and USA.
3. "A VHDL Synthesis Primer", J. Bhaskar, BSP, 2003.

ERD3105 EMBEDDED and REAL TIME SYSTEMS

Unit 1

Introduction to Embedded Systems: Categories of embedded systems, overview of embedded system architecture; specialties of embedded systems, recent trends in embedded systems. Communication interfaces: RS232/UART RS 422/RS485.

Unit 2

Survey of Software Architectures: Round Robin, Round Robin with Interrupts, Function-Queue-Scheduling Architecture, RTOS Architecture, Architecture selection. Introduction to RTOS – Tasks and Task States, Tasks and Data, Semaphores and Shared Data, More Operating System Services – Message Queues, Mailboxes, and Pipes, Timer Functions, Events, Memory Management, Interrupt Routines in an RTOS Environment.

Unit 3

Basic Design Using an RTOS: Principles, Encapsulating Semaphores and Queues, Hard Real-Time Scheduling Considerations, Saving Memory Space, Saving Power.

Unit 4

Embedded Software Development Tools – Host and Target Machines, Linker/Locators for Embedded Software, Getting Embedded Software into the Target System. Debugging Techniques - Testing on Your Host Machine, Instruction Set Simulators, The assert Macro using Laboratory Tools.

Unit 5

Writing Software for Embedded Systems: The Compilation Process, Native versus Cross-Compilers, Runtime Libraries, Writing a Library, Using alternative Libraries, Using a standard Library, Porting Kernels, C extensions for Embedded Systems, Downloading. Emulation and debugging techniques; Buffering and Other Data Structures: What is a buffer? Linear Buffers, Directional Buffers, Double Buffering, Buffer Exchange, Linked Lists, FIFOs, Circular Buffers, Buffer Under run and Overrun, Allocating Buffer memory, Memory Leakage. Memory and Performance Trade-offs

TEXT BOOKS

1. "Embedded /Real time systems: Concepts, Design and Programming", Dr. K. V. K. K. Prasad, Dream Tech Press, New Delhi, 2003.
2. "Embedded Software Primer", David Simon, Addison-Wesley, 1999.

REFERENCES

1. "Introduction to Embedded Systems", Raj Kamal, TMS, Tata McGraw Hill Publications, 2002.
2. "Embedded System Design – A Unified Hardware/Software Introduction", Frank Vahid, Tony D. Givargis, John Wiley & Sons, Inc. 2002.
3. "Embedded Microcomputer Systems" Jonathan W. Valvano, Brooks / Cole, Thompson Learning.
4. "Embedded System Design – Introduction to Processes, Tools, Techniques", Arnold S Burger, CMP Books.

ERD3106 DESIGNING WITH MICROCONTROLLERS

Unit 1

8-Bit Microcontrollers: A popular 8-bit microcontroller, Architecture: CPU Block diagram, Memory Organization, Program memory, Data Memory, Interrupts. Peripherals**:** Timers, Serial Port, I/O Port. Programming: Addressing Modes, Instruction Set, Programming, Comparison of various families of 8-bit Microcontrollers.

16-Bit Microcontrollers: A popular 16-bit Microcontroller. Architecture**:** CPU Block diagram, Memory, Special Function Registers. Comparison of different Microprocessor/Microcontroller architectures

Unit 2

16-Bit Microcontroller Peripherals: High Speed Input, High Speed Output, Interrupts, ADC, PWM, Timers, Watch-Dog Timer, Serial Port, I/O Port. Programming, Addressing Modes, Instruction Set. Comparison of various families of 16-bit Microcontrollers.

Multiple PWM Generation using High Speed Output.

Unit 3

Microcontroller based System Design: Case study with reference to a popular 8/16-bit Microcontroller. A typical application design, from requirement analysis through concept design, detailed hardware and software design using 8-bit and 16-bit Microcontrollers. Timing Analysis

Unit 4

Design, Development and Debugging Tools for Microcontroller based Systems: Software tools like Cross assembler, compiler, debuggers, simulators and hardware tools like In-Circuit Emulators (ICE), Emulators, Logic Analyzers etc.

Unit 5

PIC Microcontroller/Any Advanced Controller: CPU Architecture, Programming and peripheral details and application.

TEXT BOOKS

1. "Embedded Microcontrollers", 1st Edition; by: Intel Hand Book.
2. "Designing with Microcontrollers", 1st Edition, John B Peatman; McGraw Hill International.

REFERENCES

1. "8051 microcontroller: Architecture, Programming & Applications", 1st Edition, Ayala Kenneth J, West Publishing Company, 1996.
2. "Microcontroller Architecture, Implementation & Programming" Kenneth Hintz & Danniel, McGraw-Hill,. New York, 1992.
3. "Programming and Customizing the 8051 microcontroller", 1st Edition, Predko, Myke; McGraw Hill International.
4. "8051 Microcontroller: Hardware, Software and Interfacing", 2nd Edition, Stewart, James W, Miao, Kai X.

ERD3107 DESIGN FOR TESTABILITY

UNIT 1

Introduction to Test and Design for Testability Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation. Logic fault models, Fault detection and redundancy, Fault equivalence and fault location.

UNIT 2

Testing for single stuck faults (SSF): Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT 3

Design for testability: Testability trade-offs, techniques. Scan architectures and testing – controllability and observability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scans standards. Compression techniques - different techniques, syndrome test and signature analysis.

UNIT 4

Built-in self-test (BIST): BIST Concepts and test pattern generation. Specific BIST Architectures- CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

UNIT 5

Memory BIST (MBIST):- Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing – Introduction to automatic in circuit testing (ICT), JTAG testing features.

TEXT BOOKS

1. "Digital Systems Testing and Testable Design", Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Jaico Publishing House, 2001.
2. "Introduction to VLSI Testing", Englehood Cliffs, Robert J. Feugate, Jr., Steven M.Mentyn, Prentice Hall,1998.

REFERENCES

1. "Design for Test for Digital ICs & Embedded Core Systems", Alfred Crouch, Prentice Hall.

ERD3202 SYSTEM-ON-CHIP DESIGN

Unit 1

System on Chip Design Process: A canonical SoC design, SoC Design Flow – Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process, System level design issues- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues; Verification Strategy, On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies.

Unit 2

Macro Design Process: Top-level macro design, Macro integration, Soft macro productization, Developing hard macros: Design issues for hard macros, Design process. System Integration with reusable macros

Unit 3

SoC Verification: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification, and Static net list verification.

Unit 4

Design of Communication Architectures For SoCs: On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, Communication architectures for energy/battery efficient systems.

Unit 5

MPSoCs: What, Why, How MPSoCs. Techniques for designing MPSoCs, Performance and flexibility for MPSoC design, MPSoC performance modeling and analysis. System-In-Package (SIP) design

TEXT BOOKS

1. "SoC Verification-Methodology and Techniques", Prakash Rashinkar, Peter Paterson and Leena Singh. Kluwer Academic Publishers, 2001.
2. "Reuse Methodology manual for System-On-A-Chip Designs", Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, second edition, 2001.

REFERENCES

1. "Design Verification: Simulation and Formal Method based Approaches', William K. Lam,Prentice Hall.
2. "System-on-a-Chip-Design and Test", Rochit Rajsuman, ISBN.
3. "Multiprocessor Systems-on-chips", A. A. Jerraya, W. Wolf, M K Publishers.
4. "The EDA HandBook", Dirk Jansen, Kluwer Academic Publishers.

ERD3203 VLSI-DSP ARCHITECTURES

Unit 1

DSP Array processor architectures, fast convolution – Cook Toom algorithm, Winograd algorithm, Iterated convolution, Cyclic convolution, algorithmic strength reduction in filters and transforms, pipelined and parallel recursive and adaptive filters

Unit 2

Scaling and round off noise, digital lattice filter structures, bit level arithmetic architectures, parallel multipliers, interleaved floor plan and bit plane based digital filters, bit serial multipliers, bit serial filter design and implementation

Unit 3

Pipelining and parallel processing – pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power, retiming, unfolding, folding transformation, register minimization techniques, Register minimization in folded architectures.

Unit 4

Synchronous wave and asynchronous pipelines, synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI design, wave pipelining, asynchronous pipelining

Unit 5

Programmable Digital Signal processors – DSP processors for mobile and wireless communications, Processors for multimedia signal processing, Multiprocessor systems

TEXT BOOKS

1. "VLSI Digital Signal Processing Systems Design and Implementation", Keshab K. Parhi, Wiley-VCH Verlag GmbH & Co. KGaA.

REFERENCES

1. "Architectures for Digital Signal Processing", Peter Pirsch, IEEE Signal Processing Magazine, Vol. 14, No. 5, Sep.
2. "DSP processor fundamentals Architectures and Features", IEEE Press Series on Signal Processing.

ERD3204 EMBEDDED SYSTEM DESIGN

Unit 1

Introduction: Embedded systems overview, Design challenge: Optimizing design metrics. Processor technology: General-purpose processors, Single-purpose processors, and Application specific processors. IC technology: Full-custom/VLSI, Semi-custom ASIC, PLD, Trends. Design Technology.

Unit 2

Custom Single-Purpose Processors: RT-level combinational components. RT-level sequential components. Custom single-purpose processor design, RT-level custom single-purpose processor design, Optimizing custom single-purpose processors, Optimizing the original program, Optimizing the FSMD, Optimizing the data path, Optimizing the FSM

General-Purpose Processors: Basic architecture, Data path, Control unit, and Memory, Pipelining, Superscalar and VLIW architectures. Application-specific instruction-set processors (ASIP's), Microcontrollers, Digital signal processors (DSP), Less-general ASIP environments, Selecting a microprocessor / General purpose processor design

Unit 3

Advanced Communication Principles: Parallel communication, Serial communication, and Wireless communication. Serial Protocols: I^2C bus, CAN bus, Fire Wire bus, USB. Parallel protocols: PCI bus, AMBA bus, Wireless protocols, IrDA, Blue tooth, IEEE 802.11.

Unit 4

Digital Camera Example: User's perspective, Designer's perspective, Specification, Informal functional specification, Non-functional specification. Executable specification. Design, Implementation 1: 8051-based design, Implementation 2: Fixed point FDCT, Implementation 3: Hardware FDCT

Unit 5

Control Systems: Open-loop and closed-loop control systems, an open-looped automobile cruise-controller, a closed-loop automobile cruise-controller, General control systems and PID controllers, Control objectives, Modeling real physical systems, Controller design, Fuzzy control. Practical Issues Related to Computer based Control, Benefits of Computer Based Control Implementations

TEXT BOOKS

1. "Embedded System Design- A Unified Hardware/Software Introduction", Frank Vahid and Tony Givargis, John Wiley & Sons, 2002.

REFERENCES

1. "Embedded Systems Design" Steve Heath, Butterworth-Heinemann.
2. "Specification and Design of Embedded systems", Gajski and Vahid, Prentice Hall

ERD3205 ADVANCED MICROPROCESSOR ARCHITECTURES

Unit 1

Introduction to general structure of advanced microprocessors, Discussions on bus architecture, instruction sets, interrupts, shared data problem, interrupt latency, memory hierarchy, pipelining and RISC principles.

Unit 2

Instruction Pipeline, Design consideration & performance models, Dependency detection and resolution, Branch handling strategies, Static and dynamic pipeline, Scheduling techniques

Unit 3

Vector processor: Memory-processor interface, Vectorization techniques, Performance issues, Advanced Pipelined Processor, Superpipelined processor, Superscalar processor: Instruction scheduling, Software pipelining, VLIW

Unit 4

Cache Memory, Organization, Cache addressing, Multilevel caches, Virtual Memory, Paged, segmented and paged organizations. Address translation: Direct page table translation, Inverted page table, Table look aside buffer, Virtual memory accessing rules

Unit 5

Overviews of some popular PC-System and Microprocessor Architectures - PCI System Architecture, PCMCIA System Architecture, Plug & Play System Architecture, Card Bus System Architecture

TEXT BOOKS

1. "Computer Architecture a quantitative approach", (International Student Edition) 3rdEdition, J. Hennessy and Patterson, Morgan Kaufmann, 2000.
2. "Advanced Microprocessors", (Computer Engineering Series) –Daniel Tabak; Mc Graw Hill.

REFERENCES

1. "Architecture of high performance computers", Volume 1- R N Ibbett and N P Topham.

ERD 3206 VLSI CIRCUIT DESIGN AND TECHNOLOGY

Unit 1

Review of Microelectronics and Introduction to MOS Technologies: (MOS, CMOS,) Technology trends and projections. Basic Electrical Properties of MOS & CMOS Circuits: Ids-Vds relationships, Threshold voltage, Pass Transistor, MOS, CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits

Unit 2

Basic IC Processing Steps: Oxidation, Diffusion, Ficks Laws, Sheet resistivity, Ion implantation, Basics of vacuum deposition, chemical deposition, high and low temperature pressure depositions, Etching techniques, standard bipolar NMOS and CMOS process sequences, techniques for process evaluation analysis, in process measurements

Unit 3

CMOS System Design: CMOS memory design – SRAM and DRAM- general VLSI system components – Arithmetic circuits in CMOS VLSI – Interconnects - resistive, capacitive, inductive parasitics – chip I/O design considerations.

Unit 4

Submicron Silicon Technology and Microprocessors: GaAs Technology, Impact of GaAs technology on Microprocessor Architecture, Comparison between GaAs and Silicon technologies

Unit 5

High Performance Digital Circuits: Domino and NORA logic - BiCMOS logic - static and dynamic behavior –Delay in BiCMOS Logic - Low power CMOS design

TEXT BOOKS

1. "Basic VLSI Design", Douglas A. Pucknell and Kamran Eshraghian, Prentice-Hall, 1994.
2. "Essentials of VLSI Circuits and Systems", K. Eshraghian et.al(3 authors) PHI of India Ltd.,2005.
3. "VLSI Technology", S.M. Sze, McGraw Hill Book Company.

REFERENCES

1. "Modern VLSI Design", 3rd Edition, Wayne Wolf, Pearson Education, fifth Indian Reprint, 2005.
2. "CMOS - Circuit Design, Layout & Simulation" Jacob Baker R., Harry W. Li & David E. Boyce,, PHI, 2000.
3. "CMOS Digital Integrated Circuits - Analysis & Design", Sung-Mo Kang & Yusuf Leblebici, MGH, Second Ed., 1999.
4. "Digital Integrated Circuits - A Design Perspective", Jan M Rabaey, Prentice Hall, 1997.
5. "Digital Integrated Circuit Design", Ken Martin, Oxford University Press, 2000.

ERD3207 HIGH SPEED DIGITAL DESIGN

Unit 1

Introduction to High-Speed Digital Design: Frequency, time and distance, Capacitance and inductance effects High seed properties of logic gates, Speed and power, Modeling of wires, Geometry and electrical properties of wires, Electrical models of wires, transmission lines, loss less LC transmission lines, lossy LRC transmission lines, special transmission lines.

Unit 2

Power Distribution and Noise: Power supply network, local power regulation, IR drops, area bonding, on chip bypass capacitors, symbiotic bypass capacitors, power supply isolation, Noise sources in digital system, power supply noise, cross talk, inter-symbol interference.

Unit 3

Signaling Convention and Circuits: Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling, terminations, transmitter and receiver circuits.

Unit 4

Timing Convention and Synchronisation: Timing fundamentals, timing properties of clocked storage elements, signals and events, open loop timing level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and metastability – PLL and DLL based clock aligners.

Unit 5

Ultra-fast VLSI Circuits and Systems: GaAs Crystal structure, Technology development, Device modeling and performance Estimation. Thermal Design, Electromagnetic compatibility.

TEXT BOOKS

1. "Digital Systems Engineering", William S. Dally & John W. Poulton, Cambridge University Press, 1998.
2. "High Speed Digital Circuits", Masakazu Shoji; Adison Wesley Publishing Company, 1996.

REFERENCES

1. "Digital Integrated Circuits: A Design perspective", Jan M, Rabaey, et all; Second Edition, 2003.
2. "Basic VLSI Design", Douglas A. Pucknell and Kamran Eshraghian, Prentice-Hall, 1994.
3. "Design for Test for Digital IC's and Embedded core Systems", Alfred L Crouch; Prentice Hall.
4. "High Speed Digital Design-A Handbook of Black Magic", Howard Johnson & Martin Graham, Prentice Hall PTR, 1993.

ERD3208 ELECTRONIC SYSTEM DESIGN

Unit 1

Introduction to Electronic System Design: Packaging & Enclosures of Electronic System, Effect of environmental factors on electronic system, Cooling in of Electronic System. Electromagnetic Compatibility (EMC): Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods for reducing interference in electronic systems.

Unit 2

Cabling of Electronic Systems: Capacitive & inductive coupling, effect of shield on capacitive, inductive and magnetic coupling, coaxial cable versus shielded twisted pair.Grounding, Balancing, Filtering & Shielding of Electronic Systems, Protection against Electrostatic Discharges (ESD): Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC.

Unit 3

Practical Analog & Mixed Signal Circuit Design Issues and Techniques: (board level only) Interpreting data sheets of various passive and active components, non-ideal behavior of passive components, over voltage effects on analog integrated circuits - amplifier input stage over voltage, amplifier output voltage phase reversal, protecting integrated circuits from ESD, amplifier guard shields, amplifier decoupling. Selection of amplifiers for data converters, Properties of a high quality instrumentation amplifier

Unit 4

Design issues affecting dc accuracy & error budget analysis in instrumentation amplifier applications. Selection of isolation amplifiers, ADC and DAC static transfer function and DC errors, AC errors in data converters and dynamic performance, Selecting an A/D Converter, Analog Signal handling for high speed and accuracy, Error budget considerations for an electronic system, Circuit layout and grounding in mixed signal system, Analog & Mixed Signal circuit and PCB design exercises

Unit 5

Practical Logic Circuit Design Issues and Techniques (board level only): Interpreting data sheets of various CMOS & BiCMOS family Logic devices, Electrical behavior (steady state & dynamic) of CMOS& BiCMOS family logic devices, JTAG/IEEE 1149.1 deigns considerations, Benefits and issues on migration of 5 volt and 3.3 volt logic to lower voltage supplies Digital circuit radiation, Digital circuit layout and grounding, PCB design guidelines for reduced EMI,. Basic design considerations for backplanes, Digital circuit & PCB design exercises

TEXT BOOKS

1. "Electronic Instrument Design", 1st edition; by: Kim R. Fowler; Oxford University Press.
2. "Noise Reduction Techniques in Electronic Systems", 2nd edition; by: Henry W. Ott; John Wiley & Sons.
3. "Digital Design Principles& Practices", 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.

REFERENCES

1. Printed Circuit Boards-Design & Technology; by: W. Bosshart; Tata McGraw Hill.
2. OrCAD Layout For Windows; Visual CADD Tutorial; Version 7.10.
3. OrCAD Layout For Windows; User's Guide; CADD Tutorial; Version 7.10.